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ANALYSIS AND DESIGN OF A HIGH-POWER S-BAND POWER AMPLIFIER FOR SATELLITE JAMMERS

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ABSTRACT:

A power amplifier in S band as a main component of satellite jammer is presented. Amplifying a noise signal with high output power and efficiency was target irrespectively of linearity, signal distortion and conductivity. A class F power amplifier with GaN HEMT transistor operating in the beginning of saturation region was the optimum choice to get Maximum out power and good efficiency with smallest power dissipation.

KEYWORDS: GaN HEMT transistor; harmonic termination; power amplifier; switched mode power amplifier; Efficiency; power added efficiency; satellite jamming; Gain; output power; stability.

INTRODUCTION:

A power amplifier (PA) is a key element in wireless communication systems and jammers. Higher efficiency is always an important goal for PA designers, as it means less cost for cooling, system stability and energy conservation. Harmonically-tuned PAs such as Class F and inverse Class F (Class F-1), can offer high efficiency via non-overlapping voltage and current waveforms [1]. Class F PA can offer high efficiency by controlling the first three harmonic impedances [2].

POWER AMPLIFIER DESIGN:

Power amplifier design depends on the application and the usage. PA design follows seven main steps as shown in Fig. 1. These steps start with Class selection, second suitable transistor chosen, and third load pull simulation, fourth the input and output matching networks design, fifth schematic of the amplifier and layout generation, six EM co-simulation, finally Gerber file generation to fabrication. The next section deeply describes the PA design steps and procedures [3].

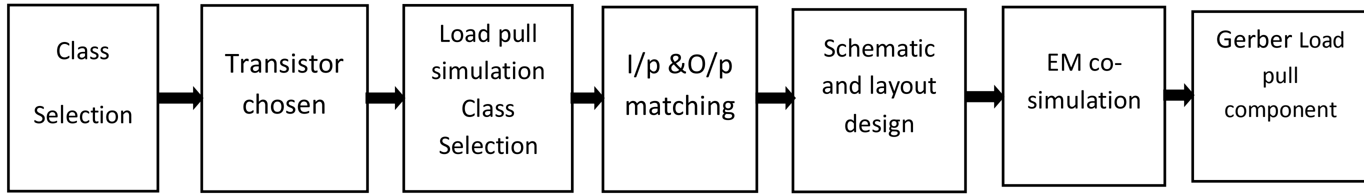

Fig.1 Power amplifier design steps design

Step 1: Class Selection

Class F is excellent for jamming application. In practical class-F designs, harmonic control up to the third harmonic provides a good balance between power efficiency, matching circuit complexity, and matching circuit losses. Class-F amplifiers are inherently nonlinear and use harmonic impedance control at the output. For high efficiency the goal is zero power dissipation and it can be achieved by short Circuit at second harmonic and open at third harmonic and to apply this topology voltage waveform at the drain which is

shorted at the odd harmonic and open in even harmonic and the drain current is shorted at even harmonic and open at odd harmonic. In an ideal class-F design, the device is cut-off for half the cycle like class B, and harmonics are created at the output circuit because the drain current is a half sinusoidal wave form. Harmonic termination impedances at the output circuit preserve the shape of the current waveform by shorting even harmonics. The drain voltage waveform is shaped to reduce overlap with the current waveform by open termination impedances at odd harmonics. There are however other important mechanisms that create harmonic frequency components including deviations from the class B bias point, nonlinear device capacitances, and nonlinear device Trans conductance [2]- [4].

Step 2: Transistor materials and industrial technology selection:

Gallium Nitride materials has high rank in the solid-state devices. High Electron Mobility Transistor had used Gallium nitride instead of Silicon in high power frequencies applications also HEMT has excellent Noise Figure. GaN materials with HEMT industrial technology is suitable for high performance and jamming applications. High power amplifier (HPA) that uses emerging technology of GaN-HEMT (Gallium Nitride High Electron Mobility Transistor) provide high output power. GaN HEMT devices with high breakdown voltage and high-power density are competent candidates for broadband high-power operation. Fortunately, the high output power of GaN devices is delivered by low device area because of high power density of this technology. High breakdown voltage allows working at high operating voltages which results in increasing optimum load impedances. So, using GaN HEMT simplifies the design of broadband PAs and enhances the efficiency. So, it will be perfect for single frequency and spot jamming application [6] [7].

Table 1 STATE-OF-THE-ART BROADBAND GaN POWER AMPLIFIERS [5]

Year	*BW[GHz]*	*Pout[W]*	*Gain[dB]*	*PAE[%]*	*Notes*
2000	2.7-3.0	250	22	25	Multi-stage
2007	DC-3.4	5	15	24	Single stage
2009	2.7-3.0	120	7.5	65	Bare die
2011	1.0-2.0	90	11	50	Single stage
2011	1.55-2.25	100	12	60	Single stage
2011	0.2-0.8	200	14.5	45	4-stage
2012	1.1-2.0	110	11	50	Single stage
2012	1.0-2.0	200	13	40	90°Power combining
2017	2.05-2.15	110	13.5	63.5	Single stage

CGH40120F transistor from Wolfspeed’s company GaN material with HEMT technology is suitable for power amplifier applications and jammers, it is the used transistor in this design. Table 1 illustrate the usage of the CGH40120F transistor in different work in several years with different applications.

Step 3: Load pull simulation:

The objective from the load pull is to know the source and load impedance values to build the input and output matching circuit, also for decreasing the errors as small as possible, and for simplicity we make the load pull for the transistor, stability circuit, and biasing circuit for the high and low voltages.

STABILITY CIRCUIT:

Two components resistance and capacitor had been built parallel to each other. These components responsible for the stability of the circuit K and B factors have the responsibility for the stability of the circuit. Which the circuit is stable when K>1 and B>0 [9]. And the stability conditions K, B had been

checked where K>1, B>0 respectively for all the band of that Include the three harmonics of interest the fundamental at 2.1GHz, second harmonic at 4.2 GHz and third harmonic at 6.3 GHz [8].

DC BIAS CONDITION FOR CLASS F PA

According to the instructions for the CGH40120F ADS model, the valid range of gate voltage Vg is from -3.8V to -2.3V so the Low bias at 3.17 V. The valid range of drain voltage Vdd is from 28V to 48V so the high bias at 32 V shows the biasing circuit for the amplifier. it consists of some capacitors each one responsible for certain frequency grounding according to the data sheet instructions [8].

THE LOAD PULL CIRCUIT:

Fig. 2 shows load pull simulation circuit to the load pull component to calculate the source and load impedances on its terminations according to the optimization goals which had been illustrated in Fig. 4 with Power added efficiency (PAE) 75 dB and out power 51.5 dBm.Fig. 3 shows the load pull components which include transistor, high voltage bias circuit, low voltage bias circuit and stability circuit.

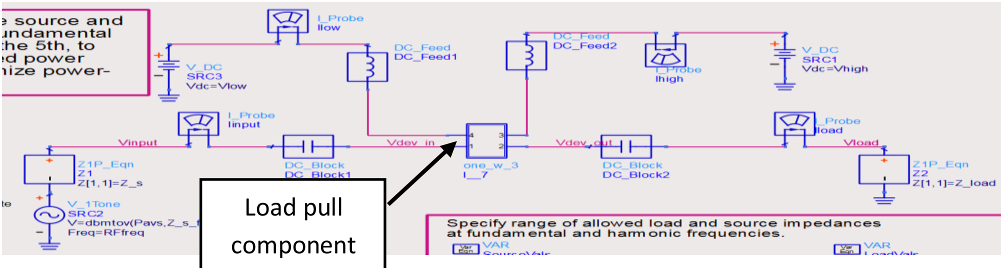

Fig.2 load pull circuit

The load-pull circuit component:

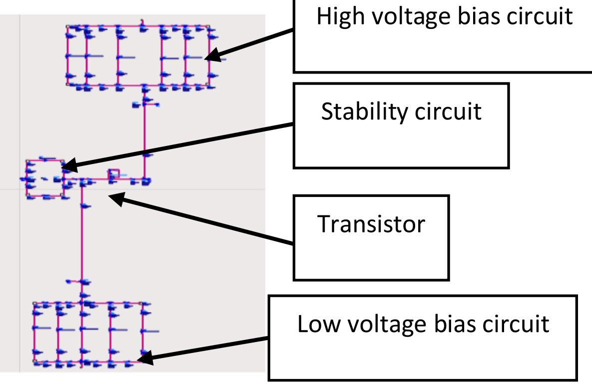

Fig.3 load pull component

With the goals:

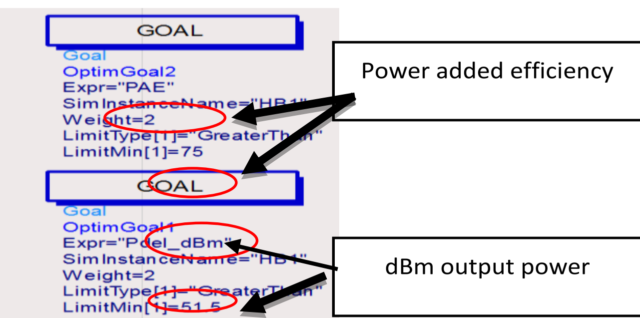

Fig.4 goals for the load pull simulation

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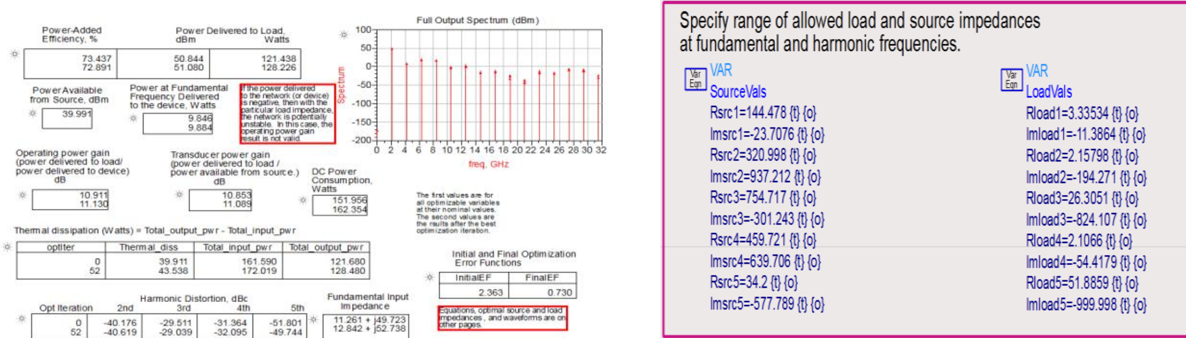

Fig.5 load pull simulation results

Fig.6 load pull impedances

Fig. 5 illustrate the optimization results which 50.844 dBm power delivered to the load, 73.437 dB PAE, 39.991 dBm source power and 11 dB gain, and these values are good and suitable to the design.

AND THE LOAD PULLS RESULTS:

Fig. 6 shows the source and load impedances for the first five harmonics which are described as real part and imaginary part for the load pull component to match it to 50 ohms.
Rsrc 1=144.478, Imsrc 1=-23.7076, Means that the source impedance for the first harmonic (Fundamental) =144.478- j 23.7076 Ohm and
Rload 3=26.3051, Im load 3=- 824.107. Means that the load impedance for the third harmonic(Fundamental) =26.3051- j 824.107 Ohm.

Step 4: The output and input matching network:

A- The output matching network:

The operating frequency or the fundamental frequency for the design is 2.1 GHz, the system is matched to 50 Ohm. The output matching network is done with three steps: third harmonic termination at 6.3 GHz, second harmonic termination 4.2 GHz and fundamental termination according to class F methodology.

(1) Third harmonic termination:

Third harmonic termination is done by terminate the transistor drain Impedance at the third harmonic frequency be open circuit.

This termination can be done by open stub with length λ3/4 with width 2 mm and length 10.66 mm this means that with this length the infinite impedance (open circuit) converts to zero impedance (short circuit) and vice versa then transmission line with length λ3/4 to convert it again to open circuit at the transistor drain as shown in Fig. 7.

(2) Second harmonic termination:

The second harmonic termination is done by terminate the transistor drain Impedance at the second harmonic to be short circuit. This termination had been done by open stub with length $\lambda_2/4$ with length 7.11 mm and width 1.26 mm. then transmission line with length λ 2/2 -λ3/4 to make the length of all the transmission line $\lambda_2/2$ because $\lambda_2/2$ don't convert the impedance just transfer the impedance as it is as shown in Fig. 7.

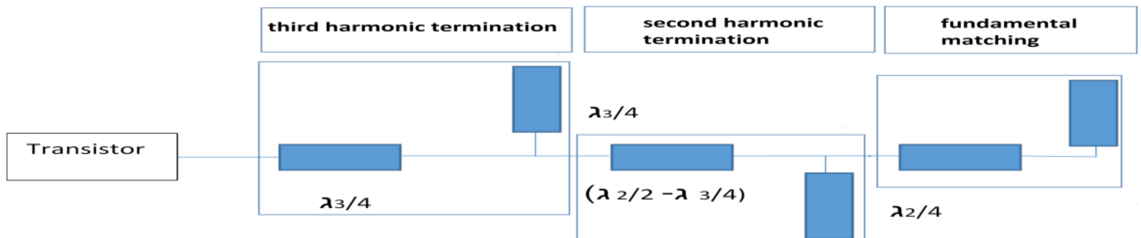

Fig.7 3rd, 2nd harmonic and fundamental matching circuit's terminations results

Table 2 Dimensions of the output matched network:

Description	Length (mm)	Width(mm)
2nd harmonic termination transmission line	6.07	1.62
2nd harmonic termination stub	7.11	1.26
3rd harmonic termination transmission line	6.01	1.62
3rd harmonic termination stub	10.66	2
Fundamental transmission line	15.66	1.62
Fundamental stub	15.47	2
And the output coupled capacitor 5.6 PF		

(3) Fundamental matching:

In single-stub tuning the two adjustable parameters are the distance, *d*, from the load to the stub position, and the value of susceptance or reactance provided by the stub. For the shunt-stub case, the basic idea is to select *d* so that the admittance, *Y*,seen considering the line at distance *d* from the load is of the form $Y0 + j B$.Then the stub susceptanceis chosen as −j B, resulting in a matched condition. For the series-stub case, the distance d is selected so that the impedance, Z, seen considering the line at a distance d from the load is of the form Z0 + j X. Then the stub reactance is chosen as −j X, resulting in a matched condition [9].

Fundamental matching network is done by open series stub with width 2 mm and length 15.47 mm and transmission line and match it with 50 Ohm as shown in Fig. 7.

B- The input matching network:

The input matching is done with two stages:

First by matching the fundamental frequency to the source load pull impedance. With the same method as the output fundamental matching with a series open stub technique. Fig. 8 shows the results of using input matching network without harmonic terminations with output power 50.33 dBm and PAE 62.6 dB.

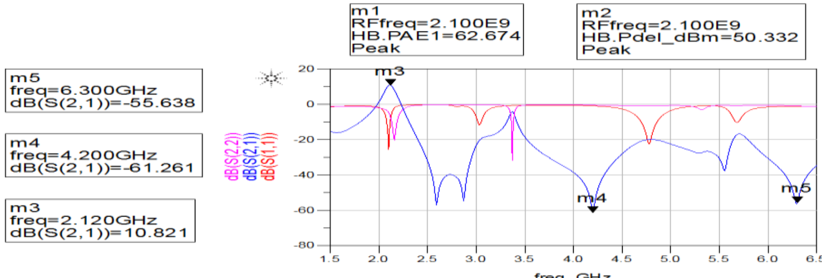

Fig.8 the input matching circuit before harmonic terminations results

The second stage is harmonic termination in the input matching network:

The Simulation is conducted on the PA with and without the input wave shaping network. PA without input wave-shaping network is only able to provide maximum PA Efficiency (PAE) of 60.31% but PA with input wave-shaping network for controlling 2fo and 3fo can provide maximum PAE of 88.97%. Almost 30% improvement in PAE is obtained after adding the input wave-shaping network [10]. PAE is improved with only from 1 to 1.5 % and the output power with 0.4 dBm by the input termination same as output matching network to. Fig. 9 shows the results of using input matching network with harmonic terminations, with output power 50.804 dBm and PAE 63.76 dB.

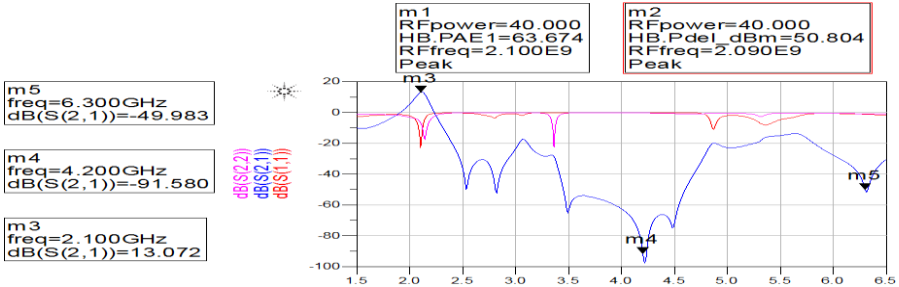

Fig.9 the input matching circuit with harmonic termination result

Table 3 shows the dimension and values of the input matched circuit.

Table 3tableof the values and diminutions of the input matched network:

Description	Length (mm)	Width(mm)
2nd harmonic termination transmission line	10.63	1.62
2nd harmonic termination stub	10.5	1. 62
3rd harmonic termination transmission line	7.2	1.62
3rd harmonic termination stub	13.15	1
Fundamental transmission line	3.4	8
Fundamental stub	17.78	1.62
And the input coupled capacitor 22 PF		

Step 5: Schematic and layout design simulation:

Whole amplifier had been simulated to gather by three main steps schematic design, layout design and EM Co-simulation.

A- SCHEMATIC DESIGN AND SIMULATION:

Amplifier is simulated with 40 dBm input signal injected to the input matched circuit with input coupling capacitor then to the stability circuit after that to the biasing circuit to bias the circuit with low bias voltage 3.17 V. Transistor gate is connected to the input network circuit and drain is connected to biasing circuit to bias the drain transistor with high voltage 32 V. then to output matched network which drive the amplified signal to coupled capacitor to the output connector.

B- SCHEMATIC SIMULATION RESULTS:

Transistor stability factors K and B was simulated with acceptable results. Also,overall dissipated power is near to zero.13 dB gain, the second harmonic terminated till -51.67 dBm and third terminated till -98.49 dBm we can detect that from the reflection at the input port S (1,1). The output power is 50.8 dBm equals to 120 watts with 40 dBm input power at 2.1 GHz. The efficiency equals 70%; power added efficiency 63.56%.

C- The layout design:
After checking the results of the schematic design and simulation layout had been generated.

Rogers Ro4350B substrate was used in the design.

Step 6: EM Co-simulation:

A- EM CO-SIMULATION DESIGN AND SIMULATION:

EM Co-simulation had been done to simulate the model of the layout in the schematic view after setting the simulation frequency and ports for all components in the schematic as shown in fig.10.

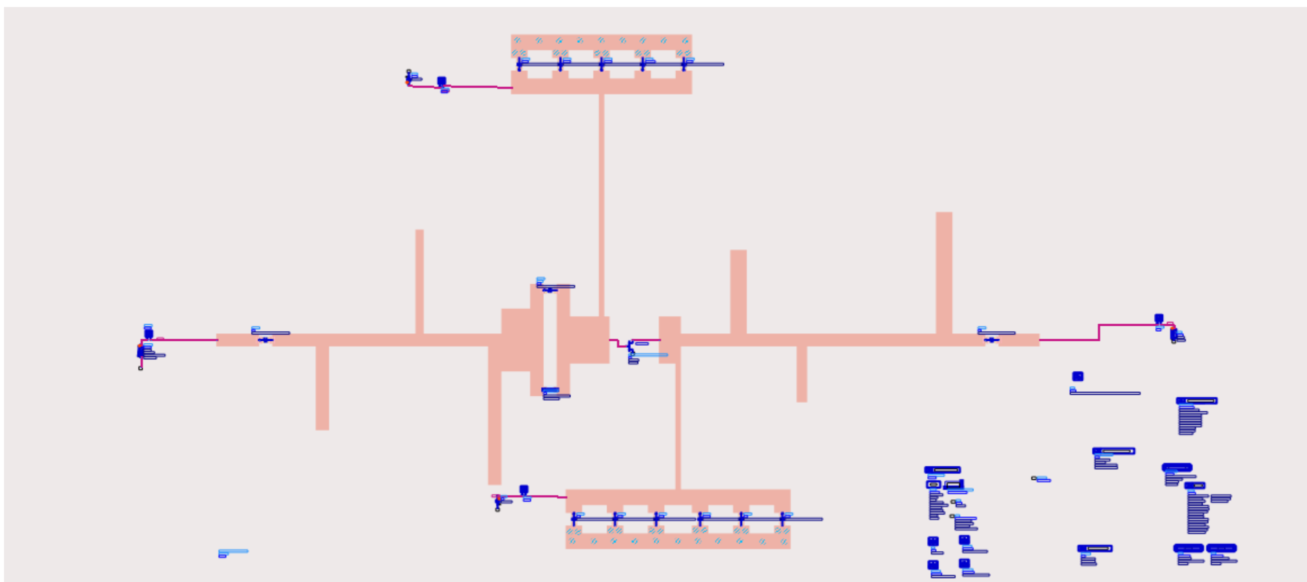

Fig.10 Em co-simulation circuit

B- EM CO-SIMULATION RESULTS:

In Fig.11 (a) the design stability had been checked and accepted.As shown in Fig. 11 (b) I ≈ 0 so P ≈ 0 from (0.15) to (0.35) and from (0.65) to (0.85). V small value so P small value from (0) to (0.15) and from (0.35) to (0.65). So, the overall dissipated power is near to zero.After EM co-simulation the gain decreased by 0.3 dB less than the schematic simulation to be 12.7 dB, the second termination changed to be -56.67 and third harmonic termination changed to be -31.12 as shown in Fig.12 (a).Fig.12(b) shows output power equals50.09 dBm (102.1 watt) which is 0.71 dBm less than the schematic simulation results.

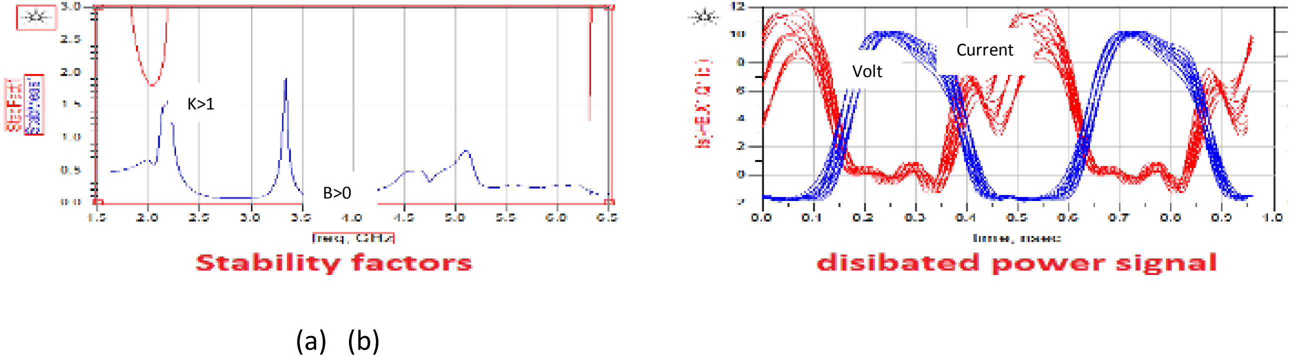

Fig.11Em co-simulation dissipated power and stability

The efficiency equals 67.245% and power added efficiency approximately equals 61.5% as shown in Fig.13(a) and

(b) respectively.

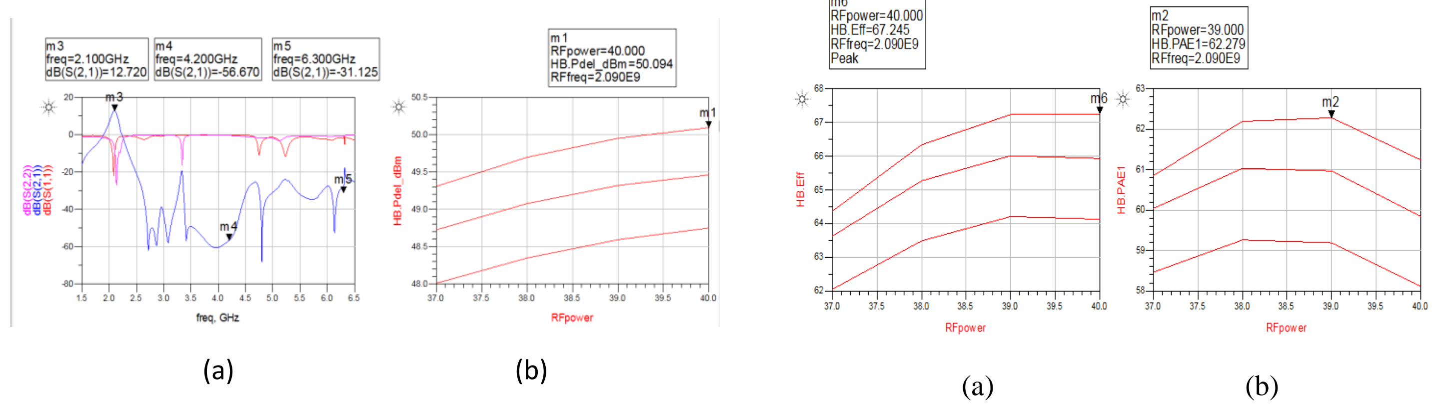

Fig.12 EM co-simulation output power, gain and harmonics

Fig.13Em co-simulation efficiency and PAE

Step 7: Gerber file generation:

From layout Gerber file, be generated to be ready for fabrication as shown in Fig. 14.

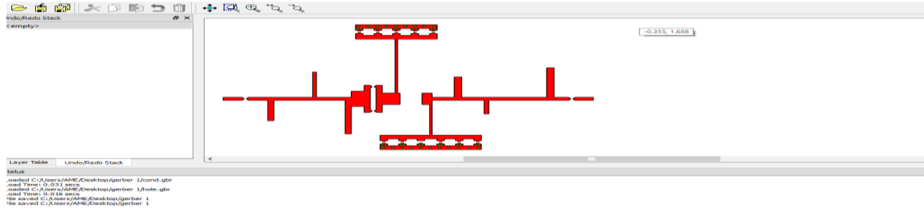

Fig.14 Gerber files generation

Finally, two files ad been generated as shown in Fig. 15.

cond.gbr	05-Jan-17 4:53 AM	GBR File	5 KB
hole.gbr	05-Jan-17 4:53 AM	GBR File	2 KB

Fig.15 Gerber files

CONCLUSIONS:

Class selection had been the starting point of the design, after that the most suitable transistor had been chosen, load pull simulation had been the done in ADS program, then the input matched network, and output matched network, schematic amplifier had been simulated after that, also layout generated, then Em co-simulation had been done, finally Gerber files had been generated from layout to the fabrication process. The output power is 50.8 dBm equals to 120 watts with 40 dBm input power at 2.1 GHz. The efficiency equals 70%; power added efficiency 63.56%.

ACKNOWLEDGEMENTS:

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